Remarks

The Applicant respectfully requests reconsideration of the present U.S. Patent application as amended herein. Claims 1 and 19 have been amended. No claims have been cancelled, added or withdrawn in this response. Thus, claims 1-6 and 19-24 remain pending in the application.

Claim Objections

Claims 19-24 were rejected under § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claim 19 was rejected for twice reciting "a first direct memory access controller." Claim 19 has been amended so that subsequent instances of the above-quoted claim term refer to "the first direct memory access controller." Thus, the Applicant respectfully requests that the rejection of claims 19-24 be withdrawn.

Claim Rejections § 103

Claims 1, 3-6, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,792,481 issued to Hoang et al. (*Hoang*) in view of U.S. Patent No. 6,418,489 issued to Mason et al. (*Mason*) in further view of U.S. Patent No. 7,051,123 issued to Baker et al. (*Baker*). The Applicant respectfully submits that claims 1, 3-6, 19, and 20 are patentable over *Hoang Mason*, and *Baker* for at least the reasons set forth below.

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The Manual of Patent Examining Procedure ("MPEP"), in § 706.02(j), states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(Emphasis added). Thus, the MPEP and applicable case law require that the Office

action establish that a combination of references teach or suggest **all of the claim**

limitations of rejected claims to sustain an obviousness rejection under 35 U.S.C. § 103.

As shown below, Applicants respectfully submit that the Office action does not establish

a *prima facie* case of obviousness.

Amended claim 1 recites:
In a controller of a computing device, the computing device comprising a system memory and a codec, a method being implemented by the controller comprising:
receiving a buffer descriptor list from a buffer descriptor list controller, the buffer descriptor list defining a plurality of buffer segments of a buffer to be read,
reading data from the buffer of the system memory **via a first interface** of the controller based, at least in part, on the buffer descriptor list,
transferring the data to the codec via a second interface of the controller,
tracking a position in the buffer from which the controller has read the data, and
writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory **via the first interface** to indicate the position in the buffer, **wherein the first interface is an isochronous interface that supports relaxed ordering rules.**

(Emphasis Added). Amended claim 19 is an apparatus claim that similarly recites "the

first direct memory access controller to **transfer data** between a system memory and a

codec via **a first interface** [and] a position controller to **update a position value** in a

direct memory access position-in-buffer (DPIB) structure located in the system memory

via the first interface … , wherein the first interface is an isochronous interface that

supports relaxed ordering rules."

> *Hoang* discloses the direct memory access (DMA) controller coupled to the
> processor and memory by the bus (Figure 1, col. 2, lines 19-38). More specifically,
> *Hoang* discloses

> Shown in FIG. 2 is DMA controller 20 of FIG. 1 in more detail. Also shown in
> FIG. 2 are FIFO 26, FIFO 24, bus 11, CODEC 28, and CODEC 30. <u>DMA
> controller 20 has</u> a receiving portion 42 and a sending portion 44. Receiving
> portion 42 comprises a buffer start address 50, a buffer end address 52, an
> interrupt period 54, a DMA control state machine 56, <u>a buffer current position 58</u>,
> an interrupt counter 60, and a missing sample counter 62.

(*Hoang*, col. 3, lines 57-63, Figure 2) (emphasis added)

> Further, *Hoang* discloses
> Similar to receiving portion 42, <u>sending portion 44</u> comprises a buffer start
> address 70, a buffer end address 72, an interrupt period 74, a DMA control state
> machine 76, <u>a buffer current position 78</u>, an interrupt counter 80, and a missing
> sample counter 82.

(*Hoang*, col. 4, lines 57-63, Figure 2) (emphasis added)

> In particular, *Hoang* discloses
> Upon initialization, the DMA control state machines 56 and 76 set buffer current
> positions 58 and 78 to the starting address in buffer start addresses 50 and 70.
> <u>Buffer current positions 58 and 78 are updated on every successful transfer</u>.

(*Hoang*, col. 4, lines 28-32) (emphasis added)

Thus, *Hoang* merely discloses updating buffer current position registers that are located in the DMA controller. In contrast, amended claim 1 recites, "**reading data** from the buffer of the system memory **via a first interface** … **writing a value** to a direct memory access position-in-buffer (DPIB) structure located in the system memory **via the first interface** … **wherein the first interface is an isochronous interface that supports relaxed ordering rules**." Amended claim 19 similarly, recites "the first direct memory access controller to **transfer data** between a system memory and a codec via **a first interface** [and] a position controller to **update a position value** in a direct memory access position-in-buffer (DPIB) structure located in the system memory **via the first interface** … , **wherein the first interface is an isochronous interface that supports relaxed ordering rules**." Thus, claims 1 and 19 each recite that the DMA data and the DPIP value are transferred via the same interface (e.g., the first interface). In addition, both claims 1 and 19 recite that "**the first interface is an isochronous interface that supports relaxed ordering rules**."

Regarding the first interface, the Office action directs the Applicant's attention to selected passages of *Mason*. The referenced passages of *Mason*, however, are merely directed to a DMA controller capable of executing FOR tasks. In particular, *Mason* states that "context information for a task" may be "stored in memory."

In contrast to *Mason*, claims 1 and 19 each recite writing a value to a DPIB structure and transferring DMA data via the same interface. *Mason* does not disclose writing a value to a DPIB structure. In addition, *Mason* does not disclose that the "context information for a task" is transferred via the same interface as the DMA data. Finally, *Mason* does not disclose that the first interface is "an isochronous interface that

supports relaxed ordering rules," as recited in claims 1 and 19. For at least the above stated reasons, *Mason* cannot cure the deficiencies of *Hoang*.

Baker is cited as teaching a number of features related to buffer descriptor lists. Whether or not *Baker* discloses the limitations cited by the Office action, a cursory review of the cited passages of *Baker*, indicates that it does not teach or suggest the above discussed features of claims 1 and 19. Because none of *Hoang, Manson,* and *Baker* teach or suggest the above-cited claim limitations, no combination of *Hoang, Manson,* and *Baker* teaches or suggests the invention as claimed in claims 1 and 19. Thus, the Applicant respectfully submits that claims 1 and 19 are patentable over the combination of *Hoang, Manson,* and *Baker*.

Claims 3-6 depend from claim 1 and claim 20 depends from claim 19. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claims 3-6 and 20 are patentable over the combination of *Hoang, Mason,* and *Baker*.

Claims 2, 23, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,792,481 issued to Hoang et al. (*Hoang*) in view of U.S. Patent No. 6,418,489 issued to Mason et al. (*Mason*) in further view of U.S. Patent No. 7,051,123 issued to Baker et al. (*Baker*) in further view of Applicant's admitted prior art (*AAPA*). The Applicant respectfully submits that claims 2, 23, and 24 are patentable over *Hoang, Mason, Baker,* and *AAPA* for at least the reasons set forth below.

AAPA is cited as teaching the use of isochronous data. Whether or not *AAPA* discloses the limitations cited by the Office action, it does not teach or suggest the above-

discussed features of claims 1 and 19. Because none of *Hoang, Mason, Baker*, and *AAPA*

teach or suggest the above-discussed claim limitations, no combination of *Hoang, Mason,*

Baker, and *AAPA* teaches or suggests the invention as claimed in claims 1 and 19. Claim

2 depends from claim 1 and claims 23 and 24 depend from claim 19. For at least the

reason that dependent claims include the limitations of the claims from which they

depend, the Applicant respectfully submits that claims 2, 23, and 24 are patentable over

Hoang, Mason, Baker, and *AAPA*.

Claims 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable

over U.S. Patent No. 6,792,481 issued to Hoang et al. (*Hoang*) in view of U.S. Patent No.

6,418,489 issued to Mason et al. (*Mason*) in further view of U.S. Patent No. 7,051,123

issued to Baker et al. (*Baker*) in further view of U.S. Patent No. 6,693,753 issued to Su et

al. (*Su*). The Applicant respectfully submits that claims 21 and 22 are patentable over

Hoang, Mason, Baker, and *Su* for at least the reasons set forth below.

Su is cited as teaching aspects of a link position counter. Whether or not *Su*

discloses the limitations cited by the Office action, a cursory review of the cited passages

of *Su* indicates that it does not teach or suggest the above-discussed features of claims 1

and 19. Because none of *Hoang, Mason, Baker* and *Su* teaches or suggests the above-

cited claim limitations, no combination of *Hoang, Mason, Baker* and *Su* teaches or

suggests the invention as claimed in claims 1 and 19. Claims 21 and 22 depend from

claim 19. For at least the reason that dependent claims include the limitations of the

claims from which they depend, the Applicant respectfully submits that claims 21 and 22

are patentable over *Hoang, Mason, Baker*, and *Su*.

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Conclusion

The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Respectfully submitted,

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